$$\text{Energy loss during turn-off} = \int_0^{t_{off}} \left(100 - \frac{100}{60} \times 10^6\, t\right)\left(\frac{200}{75} \times 10^6\, t\right) dt$$

$$= 0.1603 \text{ watt–sec}$$

Total energy loss in one cycle

$$= 0.1067 + 0.1603 = 0.267 \text{ W–sec}$$

Average power loss in transistor

$$= \text{switching frequency} \times \text{energy loss in one cycle}$$

∴ Allowable switching frequency,

$$f = \frac{300}{0.267} = 1123.6 \text{ Hz}$$

2.4. POWER MOSFETs

A metal-oxide-semiconductor field-effect transistor (MOSFET) is a recent device developed by combining the areas of field-effect concept and MOS technology.

A power MOSFET has three terminals called drain, source and gate in place of the corresponding three terminals collector, emitter and base for BJT. The circuit symbol of power MOSFET is as shown in Fig. 2.11 (*a*). Here arrow indicates the direction of electron flow. A BJT is a current controlled device whereas a power MOSFET is a voltage-controlled device. As its operation depends upon the flow of majority carriers only, MOSFET is a unipolar device. The control signal, or base current in BJT is much larger than the control signal (or gate current) required in a MOSFET. This is because of the fact that gate circuit impedance in MOSFET is extremely high, of the order of 10^9 ohm. This large impedance permits the MOSFET gate to be driven directly from microelectronic circuits. BJT suffers from second breakdown voltage whereas MOSFET is free from this problem. Power MOSFETs are now finding increasing applications in low-power high frequency converters.

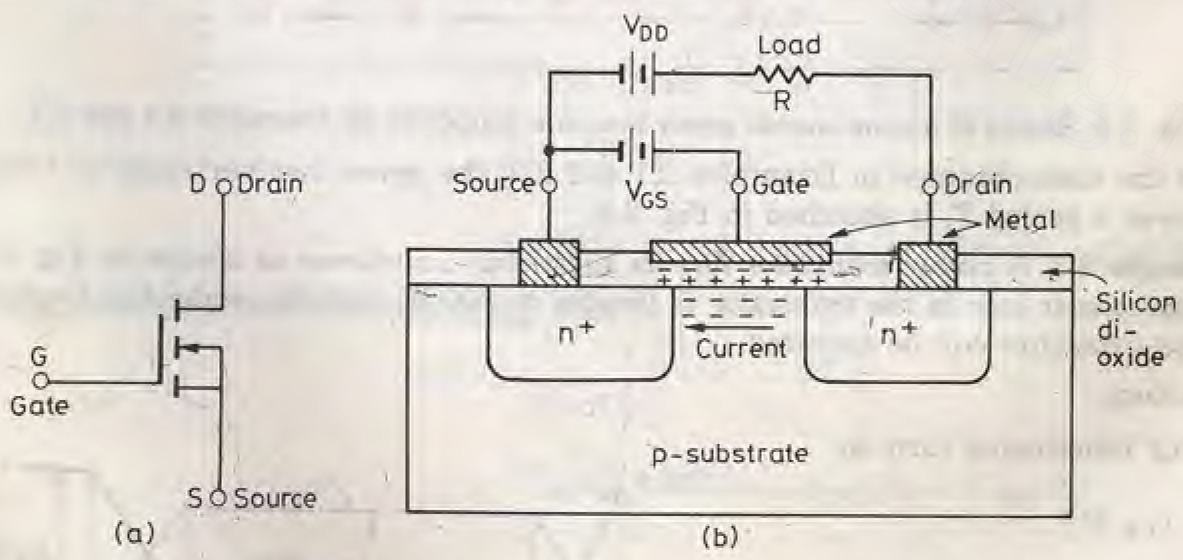


Fig. 2.11. *N*-channel enhancement power MOSFET
(*a*) circuit symbol and (*b*) its basic structure.

Power MOSFETs are of two types ; *n*-channel enhancement MOSFET and *p*-channel enhancement MOSFET. Out of these two types, *n*-channel enhancement MOSFET is more common because of higher mobility of electrons. As such, only this type of MOSFET is studied in what follows.

A simplified structure of n-channel planar MOSFET of low power rating is shown in Fig. 2.11 (*b*). On p-substrate (or body), two heavily doped n^+ regions are diffused as shown. An insulating layer of silicon dioxide (SiO_2) is grown on the surface. Now this insulating layer is etched in order to embed metallic source and drain terminals. Note that n^+ regions make contact with source and drain terminals as shown. A layer of metal is also deposited on SiO_2 layer so as to form the gate of MOSFET.

When gate circuit is open, no current flows from drain to source and load because of one reverse-biased n^+–p junction. When gate is made positive with respect to source, an electric field is established as shown in Fig. 2.11 (*b*). Eventually, induced negative charges in the p-substrate below SiO_2 layer are formed. These negative charges, called electrons, form n-channel and current can flow from drain to source as shown by the arrow. If V_{GS} is made more positive, n-channel becomes more deep and therefore more current flows from D to S. This shows that drain current I_D is enhanced by the gradual increase of gate voltage, hence the name enhancement MOSFET.

The main disadvantage of n-channel planar MOSFET of Fig. 2.11 (*b*) is that conducting n-channel in between drain and source gives large on-state resistance. This leads to high power dissipation in n-channel. This shows that planar MOSFET construction of Fig. 2.11 (*b*) is feasible only for low-power MOSFETs.

The constructional details of high power MOSFET are illustrated in Fig. 2.12. In this figure is shown a planar diffused metal-oxide-semiconductor (DMOS) structure for n-channel

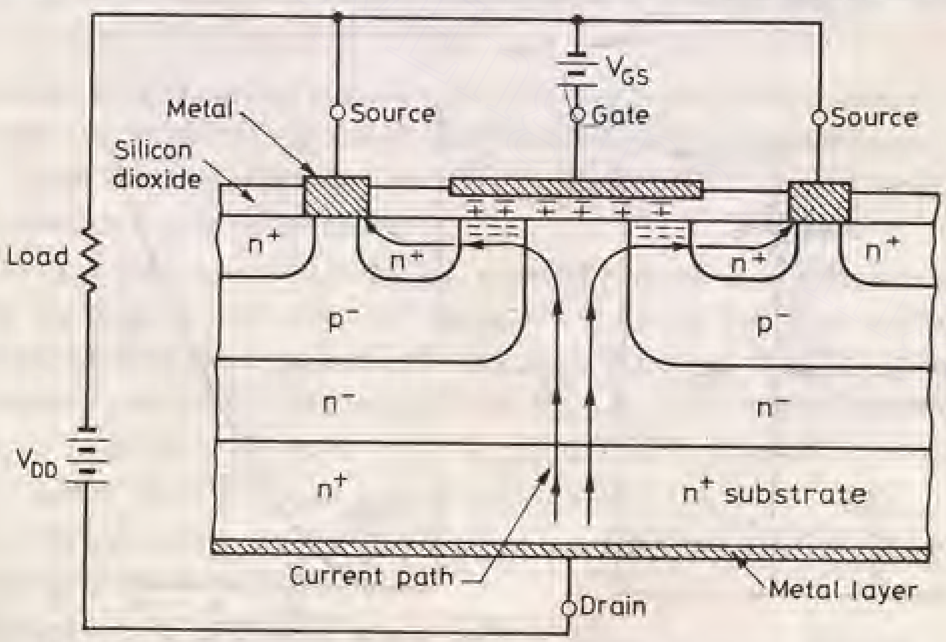


Fig. 2.12. Basic structure of a n-channel DMOS power MOSFET.

which is quite common for power MOSFETs. On n^+ substrate, high resistivity n^- layer is epitaxially* grown. The thickness of n^- layer determines the voltage blocking capability of the device. On the other side of n^+ substrate, a metal layer is deposited to form the drain terminal. Now p^- regions are diffused in the epitaxially grown n^- layer. Further, n^+ regions are diffused in p^- regions as shown. As before, SiO_2 layer is added, which is then etched so as

* A mixture of silicon atoms and pentavalent atoms, deposited on wafer, forms a layer of n-type semiconductor on heated surface. This layer is called expitaxial layer.

to fit metallic source and gate terminals. A power MOSFET actually consists of a parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

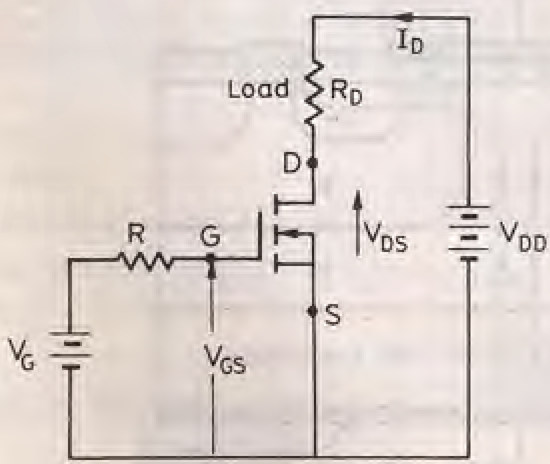
When gate circuit voltage is zero, and V_{DD} is present , $n^- - p^-$ junctions are reverse biased and no current flows from drain to source. When gate terminal is made positive with respect to source, an electric field is established and electrons form n-channel in the p^- regions as shown. So a current from drain to source is established as indicated by arrows. With gate voltage increased current I_D also increases as expected. Length of n-channel can be controlled and therefore on-resistance can be made low if short length is used for the channel.

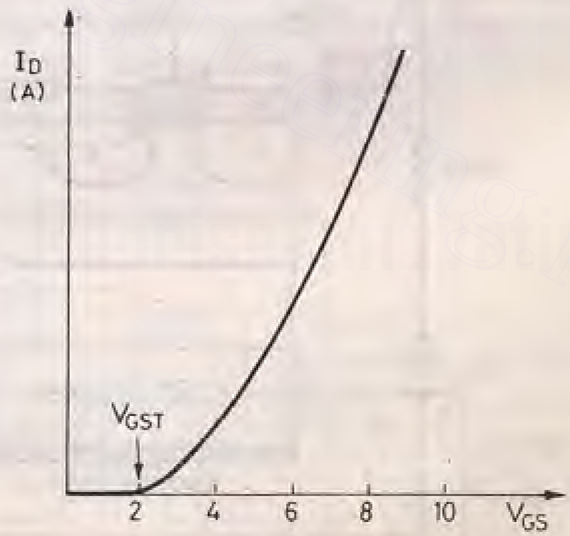
Power MOSFET conduction is due to majority carriers, therefore, time delays caused by removal or recombination of minority carriers are eliminated. Thus, power MOSFET can work at switching frequencies in the megahertz range.

2.4.1. MOSFET Characteristics

The static characteristics of power MOSFET are now described briefly. The basic circuit diagram for n-channel power MOSFET is shown in Fig. 2.13 (a) where voltages and currents are as indicated.

(a) **Transfer characteristics.** This characteristic shows the variation of drain current I_D as a function of gate-source voltage V_{GS}. Fig. 2.13 (b) shows typical transfer characteristic for n-channel power MOSFET. It is seen that there is threshold voltage V_{GST} below which the device is off. The magnitude of V_{GST} is of the order of 2 to 3 V.





(a) (b)

Fig. 2.13. (a) N-channel power MOSFET circuit diagram and (b) its typical transfer characteristic.

(b) **Output characteristics.** Power MOSFET output characteristics shown in Fig. 2.14 indicate the variation of drain current I_D as a function of drain-source voltage V_{GS} as a parameter. For low values of V_{DS}, the graph between $I_D - V_{DS}$ is almost linear ; this indicates a constant value of on-resistance $R_{DS} = V_{DS}/I_D$. For given V_{GS}, if V_{DS} is increased, output characteristic is relatively flat indicating that drain current is nearly constant. A load line intersects the output characteristics at A and B. Here A indicates fully-on condition and B fully-off state. Power MOSFET operates as a switch either at A or at B just like a BJT.

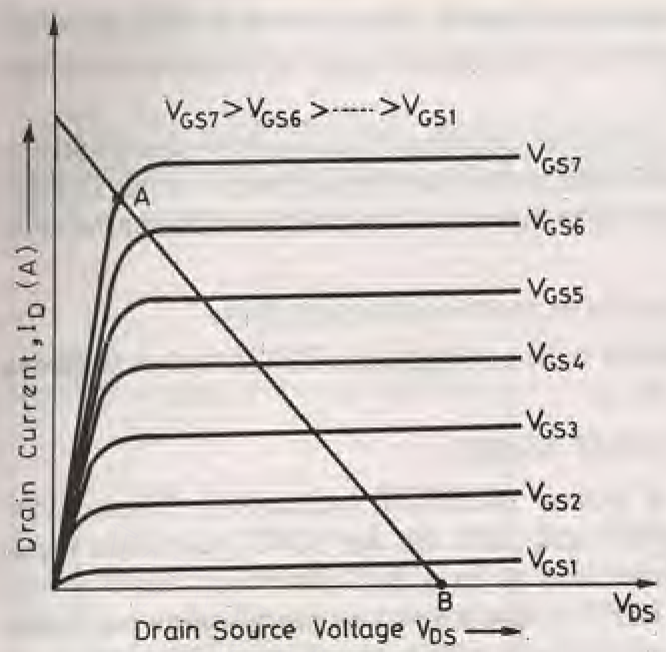


Fig. 2.14. Output characteristics of a power MOSFET.

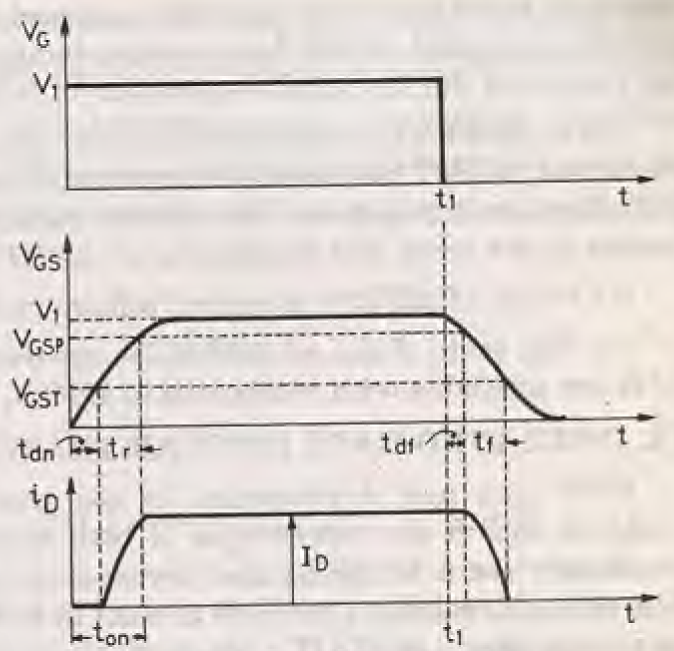


Fig. 2.15. Switching waveforms for power MOSFET.

(*c*) **Switching characteristics.** The switching characteristics of a power MOSFET are influenced to a large extent by the internal capacitance of the device and the internal impedance of the gate drive circuit. At turn-on, there is an initial delay t_{dn} during which input capacitance charges to gate threshold voltage V_{GST}. Here t_{dn} is called *turn-on delay* time.

There is further delay t_r, called *rise time*, during which gate voltage rises to V_{GSP}, a voltage sufficient to drive the MOSFET into on state. During t_r, drain current rises from zero to full on current I_D. Thus, the total turn-on time is $t_{on} = t_{dn} + t_r$. The turn-on time can be reduced by using low-impedance gate drive source.

As MOSFET is a majority carrier device, turn-off process is initiated soon after removal of gate voltage at time t_1. The turn-off delay time, t_{df}, is the time during which input capacitance discharges from overdrive gate voltage V_1 to V_{GSP}. The *fall time*, t_f is the time during which input capacitance discharges from V_{GSP} to threshold voltage. During t_f, drain current falls from I_D to zero. So when $V_{GS} \le V_{GST}$, MOSFET turn-off is complete. Switching waveforms for a power MOSFET are shown in Fig. 2.15.

Power MOSFETs are very popular in switched mode power supplies. They are, at present, available with 500 V, 140 A ratings.

2.4.2. Comparison of MOSFET with BJT

Power MOSFET has several features different from those of BJT. These are outlined as under :

(*i*) Power MOSFET has lower switching losses but its on-resistance and conduction losses are more. A BJT has higher switching losses but lower conduction loss. So at high frequency applications, power MOSFET is the obvious choice. But at lower operating frequencies (less than about 10 to 30 kHz), BJT is superior.

(*ii*) MOSFET is voltage controlled device whereas BJT is current controlled device.

(*iii*) MOSFET has positive temperature coefficient for resistance. This makes parallel operation of MOSFETs easy. If a MOSFET shares increased current initially, it heats up